FIG. 1A

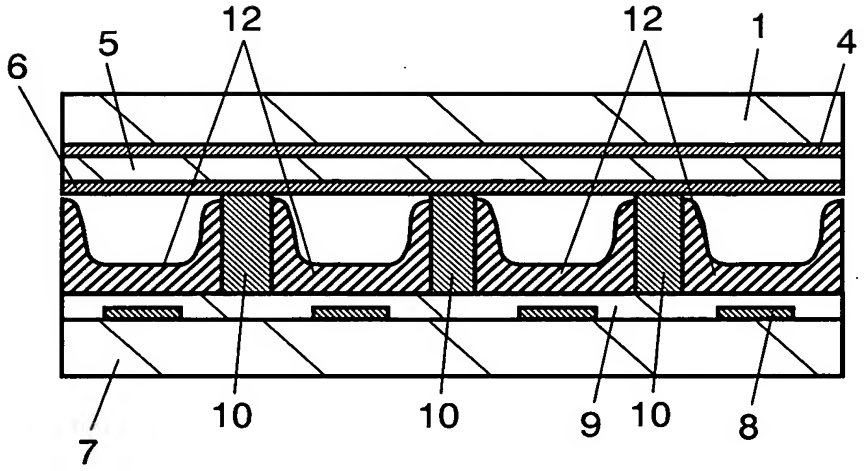

FIG. 1B

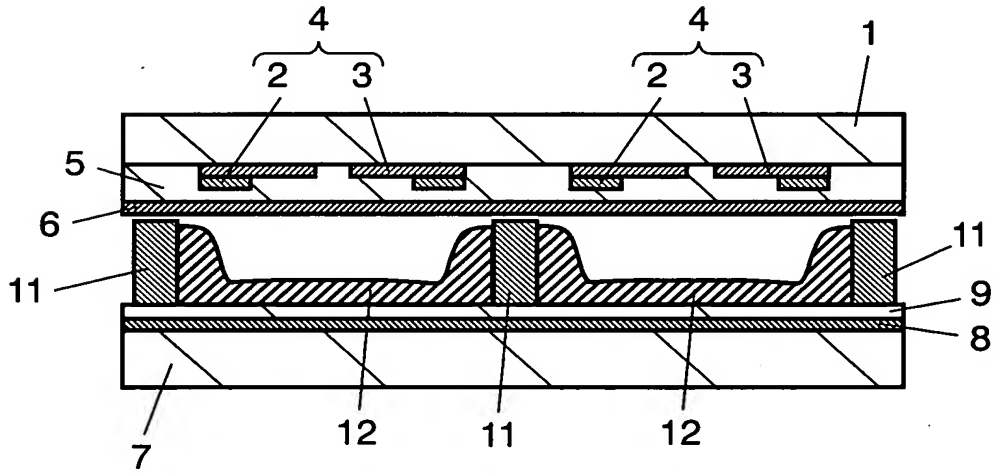

FIG. 2

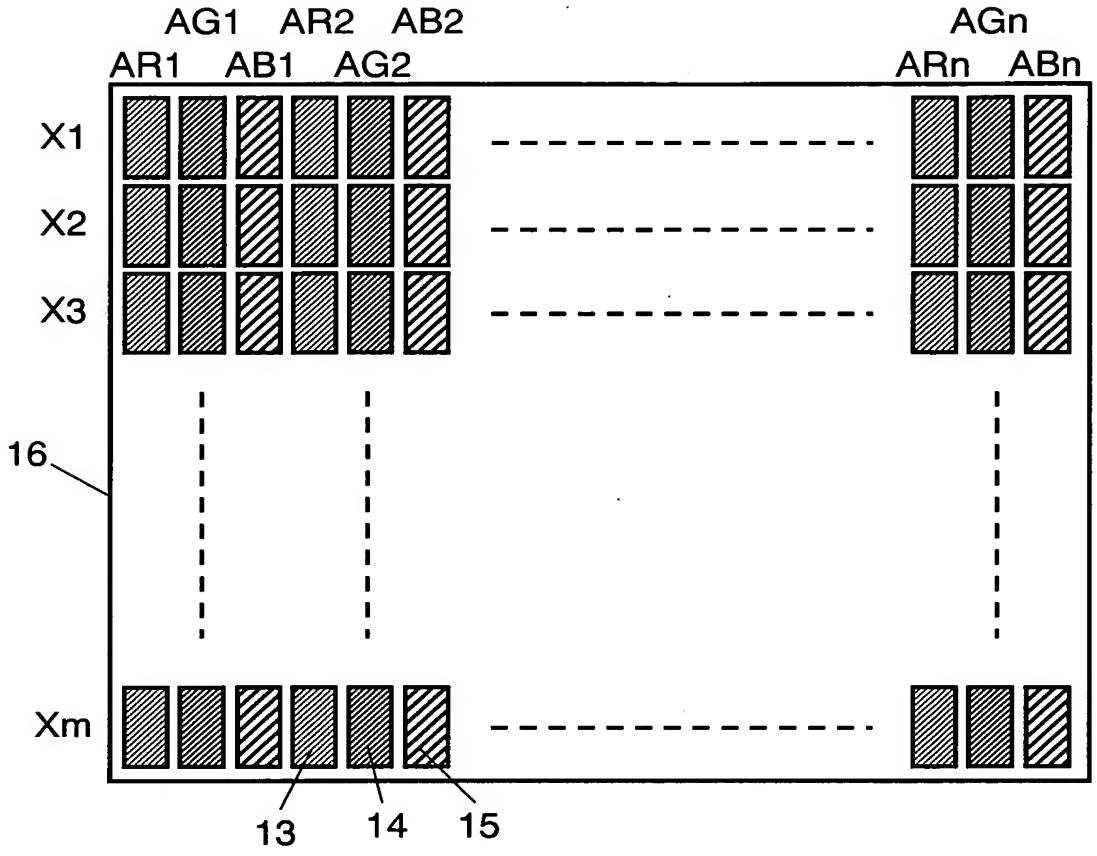
AG1
AR2
AB2
AGn
AR1
AB1
AG2
ARn
ABn
X1
X2
X3
16
Xm
13
14
15

FIG. 3

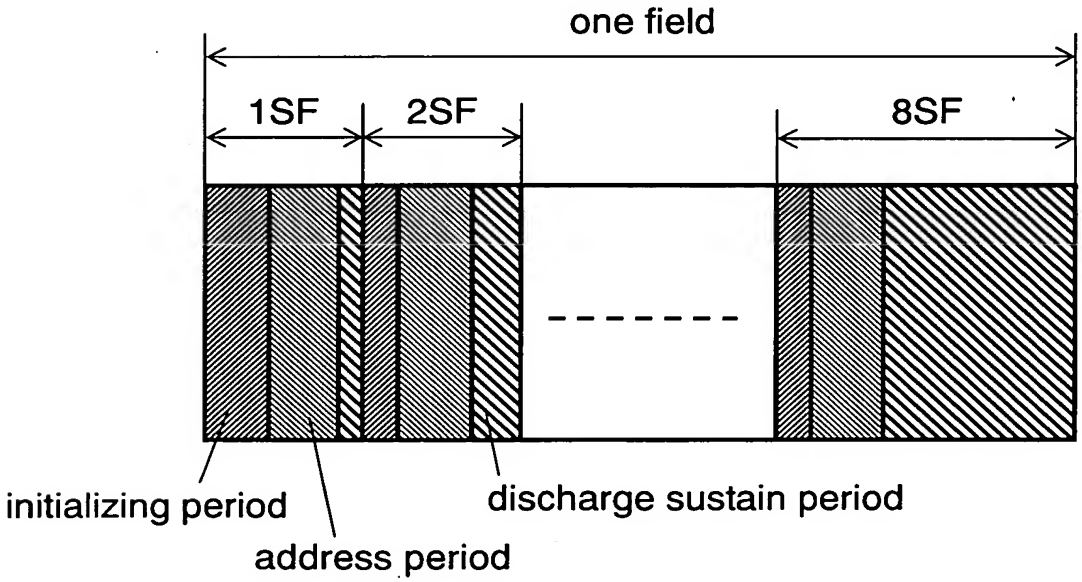
one field
1SF
2SF
8SF
initializing period
address period
discharge sustain period

FIG. 4

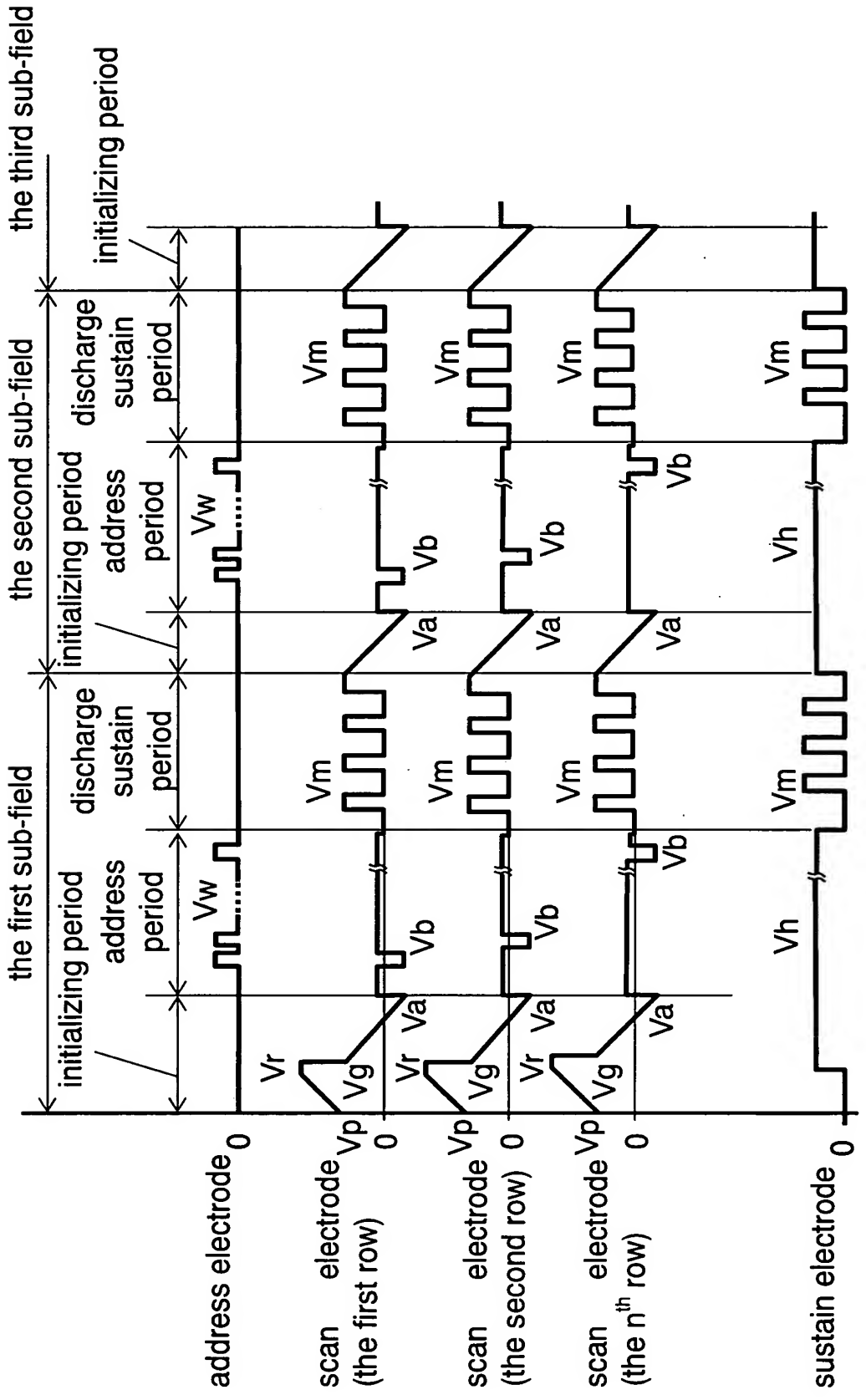
the first sub-field
the second sub-field
the third sub-field
initializing period
address period
discharge sustain period
initializing period
address period
discharge sustain period
initializing period
address electrode
scan electrode (the first row)
scan electrode (the second row)
scan electrode (the n^th row)
sustain electrode
Vr
Vg
Va
Vb
Vw
Vm
Vh
Vp
0

FIG. 5

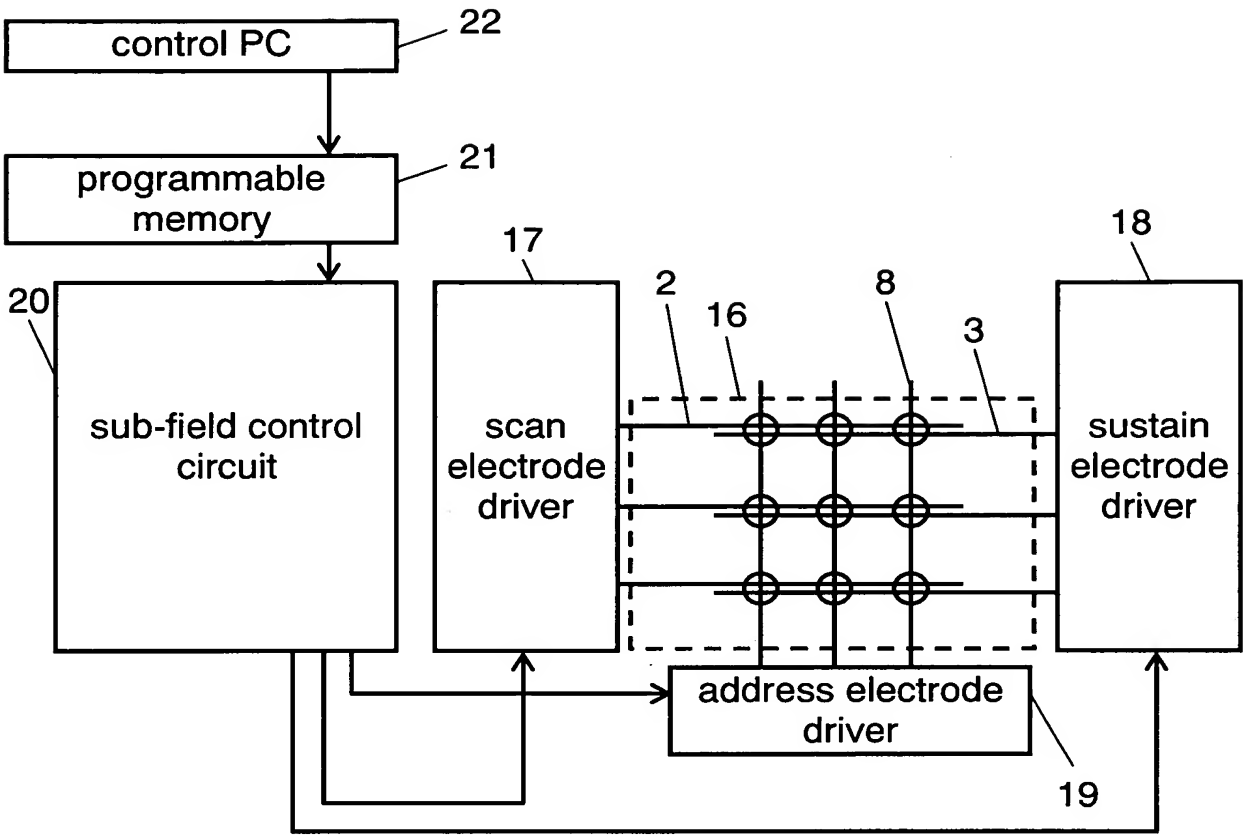
control PC
22
programmable memory
21
20
sub-field control circuit
17
scan electrode driver
2
16
8
3
18
sustain electrode driver
address electrode driver
19

FIG. 6

R-cell

rows	1SF	2SF	3SF	4SF	5SF	6SF	7SF	8SF
odd-rows	○	○	○	×	×	×	×	×
even-rows	×	×	×	×	×	×	×	×

G-cell

rows	1SF	2SF	3SF	4SF	5SF	6SF	7SF	8SF
odd-rows	×	×	×	○	×	×	×	×
even-rows	×	×	×	×	×	×	×	×

B-cell

rows	1SF	2SF	3SF	4SF	5SF	6SF	7SF	8SF
odd-rows	○	○	○	×	×	×	×	×
even-rows	×	×	×	×	×	×	×	×

○ : address pulse is applied

× : address pulse is not applied

FIG. 7

R-cell

rows	1SF	2SF	3SF	4SF	5SF	6SF	7SF	8SF
odd-rows	×	×	×	×	×	×	×	×
even-rows	×	×	×	×	×	×	×	×

G-cell

rows	1SF	2SF	3SF	4SF	5SF	6SF	7SF	8SF
odd-rows	○	○	○	×	×	×	×	×
even-rows	×	×	×	○	×	×	×	×

B-cell

rows	1SF	2SF	3SF	4SF	5SF	6SF	7SF	8SF
odd-rows	×	×	×	×	×	×	×	×
even-rows	×	×	×	×	×	×	×	×

○ : address pulse is applied

× : address pulse is not applied

FIG. 8

R-cell

rows	1SF	2SF	3SF	4SF	5SF	6SF	7SF	8SF
odd-rows	○	○	○	×	×	×	×	×
even-rows	×	×	×	×	×	×	×	×

G-cell

rows	1SF	2SF	3SF	4SF	5SF	6SF	7SF	8SF
odd-rows	×	×	×	×	×	×	×	×
even-rows	×	×	×	○	×	×	×	×

B-cell

rows	1SF	2SF	3SF	4SF	5SF	6SF	7SF	8SF
odd-rows	○	○	○	×	×	×	×	×
even-rows	×	×	×	×	×	×	×	×

○ : address pulse is applied

× : address pulse is not applied

Reference numerals in the drawings

2: scan electrode
3: sustain electrode
4: display electrode
8: address electrode
13: R-cell
14: G-cell
15: B-cell